SOLID-STATE IMAGING APPARATUS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a solid-state imaging apparatus with an electronic shutter function and, in particular, to a solid-state imaging apparatus which discharges a carrier toward a substrate.

[0003] 2. Description of the Related Art

[0004] Hitherto, a solid-state imaging apparatus has used a so-called a vertical overflow drain (VOFD) in which a voltage is applied to a semiconductor substrate to discharge a carrier of a photoelectric conversion element to control accumulation time, thereby realizing an electronic shutter function. Particularly, the function is often used in a CCD solid-state imaging apparatus.

[0005] Japanese Patent Application Laid-Open No. 2005-166731 proposes a solid-state imaging apparatus which causes a MOS solid-state imaging apparatus to operate a VOFD function to realize an electronic shutter function.

[0006] A structure shown in Japanese Patent Application Laid-Open No. 2005-166731 leaves room for improvement in the following respects.

[0007] Applying a high voltage to an N-type semiconductor substrate to realize the VOFD function significantly varies a potential in a buried layer due to a capacitive coupling between the substrate and a P-type buried layer acting as a potential barrier. This may significantly vary a potential in a P-type semiconductor region electrically connected to the buried layer. Particularly, if a pixel has a carrier accumulating region for temporarily holding a signal carrier from a photoelectric conversion region, a P-type semiconductor region forming a potential barrier is provided in the vicinity of the carrier accumulating region to effectively accumulate the carriers to significantly vary a potential in the P-type semiconductor region. As a result, the carriers accumulated in a carrier accumulation region leak toward the substrate to vary the amount of accumulated carriers, which may degrade image quality.

[0008] Variation in potential in the P-type semiconductor region forming the potential barrier can result also from variation in potential of a source and a drain in the operation of each MOS transistor. This is because a potential of a P-type well being a back gate of the MOS transistor capacitively coupled with the source or the drain varies to vary a potential in the P-type semiconductor region forming the potential barrier electrically connected to the well.

[0009] The present invention has been made in view of the above problem and an object of the present invention is to moderate variation in the amount of accumulated carriers when the VOFD function is used to realize an electronic shutter function, thereby performing a high image-quality photographing.

SUMMARY OF THE INVENTION

[0010] According to the present invention, a solid-state imaging apparatus having a semiconductor substrate of a first conductivity type, and a plurality of pixels arranged in a pixel region of the semiconductor substrate, each pixel including a photoelectric conversion region and an amplifying transistor for amplifying a signal based on a signal carrier generated in the photoelectric conversion region and for outputting an amplified signal, performing a vertical over flow drain operation, wherein the pixel region includes: a first semiconductor region of the first conductivity type for forming a part of the photoelectric conversion region; a second semiconductor region of the first conductivity type for accumulating the carriers generated in the photoelectric conversion region; a third semiconductor region of a second conductivity type arranged under the second semiconductor region, as a potential barrier holding the accumulated carriers in the second semiconductor region; a fourth semiconductor region of the second conductivity type extending between the first semiconductor region and the semiconductor substrate, and between the third semiconductor region and the semiconductor substrate; and a first voltage supply portion for supplying a reference voltage to the third semiconductor region, wherein the first voltage supply portion includes a fifth semiconductor region of the second conductivity type arranged in the pixel region, and a first electrode connected to the fifth semiconductor region.

[0011] Further features of the present invention will become apparent from the following description of exemplary embodiments with reference to the attached drawings.

[0012] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. **1** is a schematic diagram for describing a first embodiment and a cross section taken along the line C-C' of FIG. **2**.

[0014] FIG. **2** is a plan view for describing the first embodiment.

[0015] FIG. **3** is an equivalent circuit for describing the first embodiment.

[0016] FIG. **4** is a schematic diagram for describing the first embodiment and a cross section taken along the line D-D' of FIG. **2**.

[0017] FIG. **5** is a potential diagram taken along the line Y-Y' of FIG. **1**.

[0018] FIG. **6** is a schematic diagram for describing a second embodiment and a cross section taken along the line C-C' of FIG. **2**.

[0019] FIG. **7** is a cross section for describing a third embodiment.

[0020] FIG. **8** is a cross section for describing a fourth embodiment.

[0021] FIGS. **9**A, **9**B and **9**C are schematic diagrams illustrating production processes for forming the solid-state imaging apparatus in the fourth embodiment.

[0022] FIG. **10** is a schematic diagram for describing a fifth embodiment and a cross section taken along the line G-G' of FIG. **13**.

[0023] FIG. **11** is a plan view for describing the fifth embodiment.

[0024] FIG. **12** is a schematic diagram for describing the fifth embodiment and a cross section taken along the line H-H' of FIG. **13**.

[0025] FIG. **13** is a plan view for describing a sixth embodiment.